Chips and Achievements

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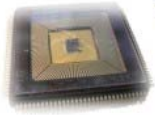
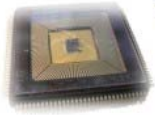
Yuan-Ze University, Taiwan



VSPS Lab.
VLSI Signal Processing Systems Laboratory

Dual-Mode TC/CC Decoder for IDD Receiver

Department of Electrical Engineering
Yuan-Ze University, Taiwan



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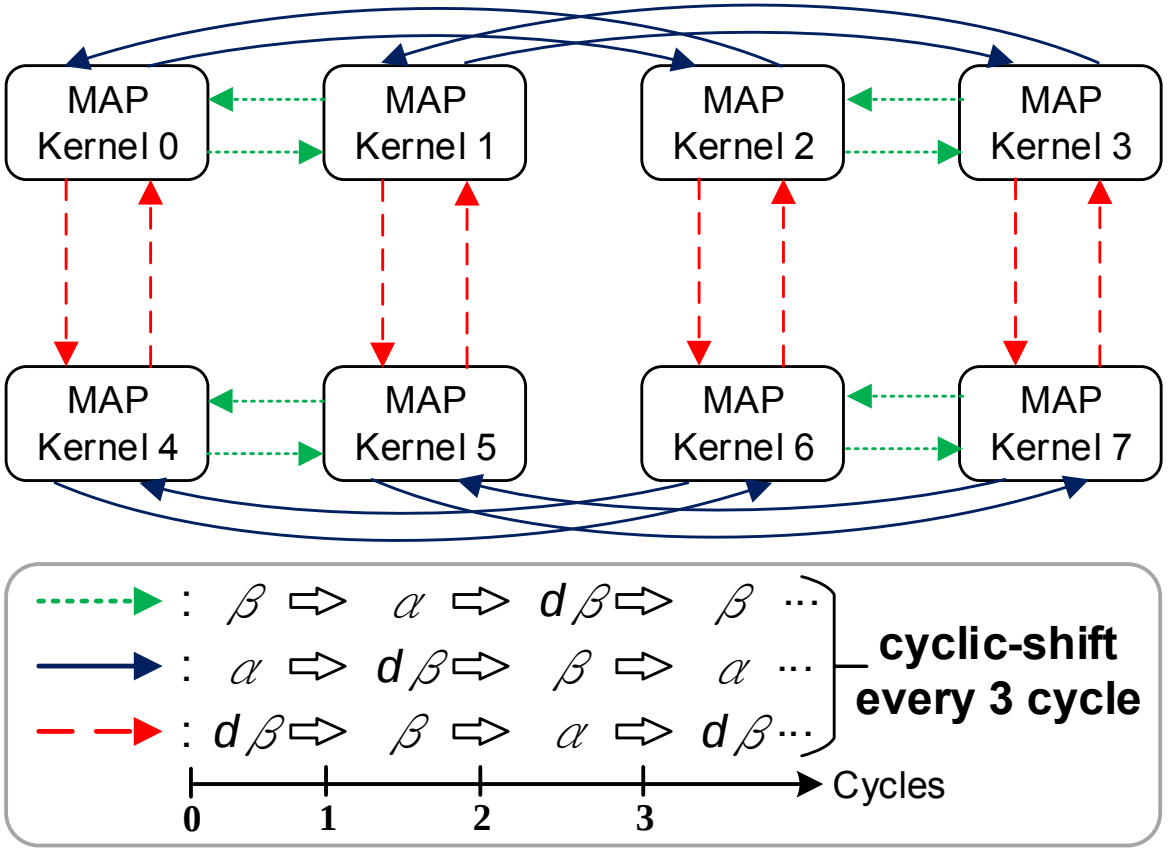
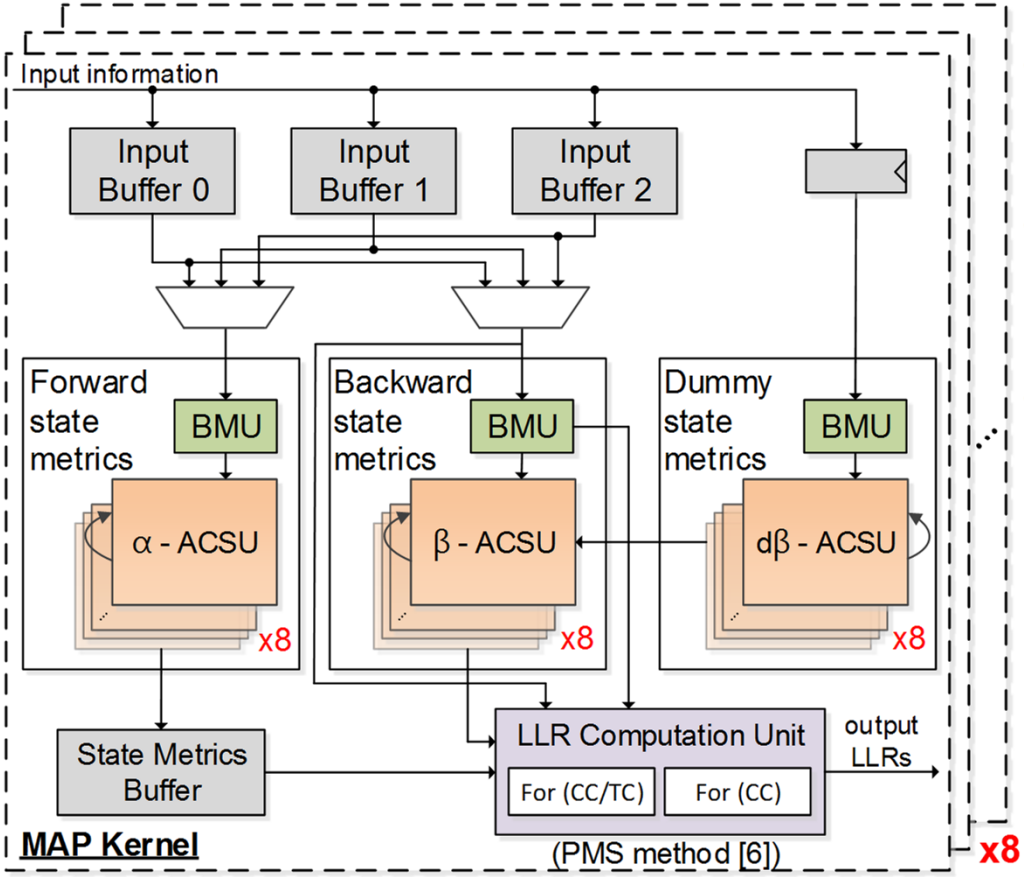
Dual-Mode TC/CC Decoder for IDD Receiver

- Global state metrics transfers between 8 parallel MAP kernels.



Proposed Decoder Architecture

- The proposed parallel dual-mode MAP decoding architecture composed of 8 MAP kernels.
  - Decode 8 blocks of 8-state TC or 1 block of 64-state CC.

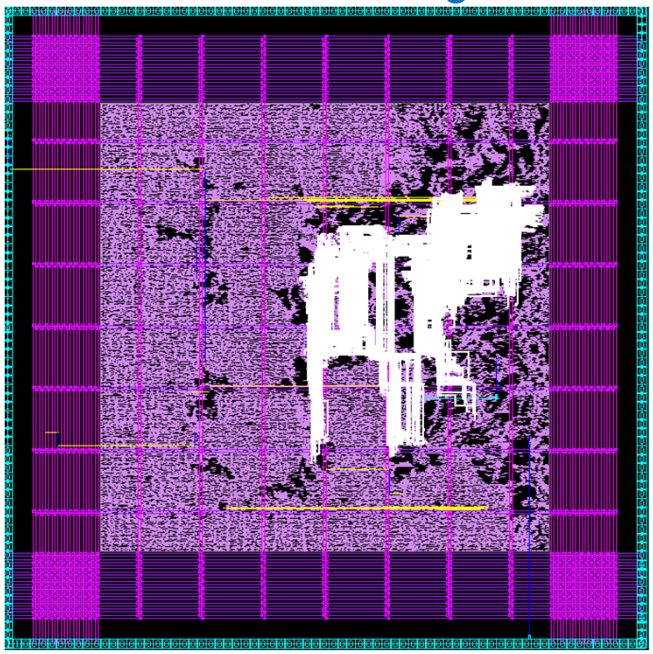


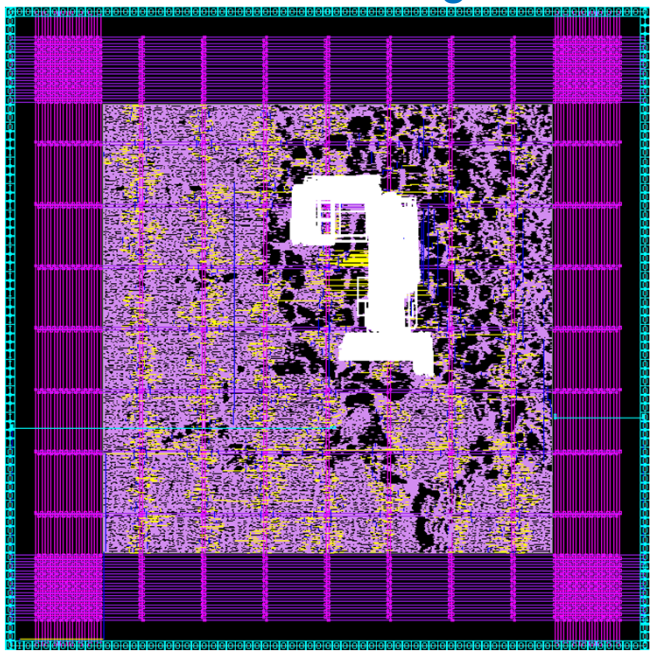
- **Branch Metrics Unit (BMU):** compute the branch metrics
- **Add-Compared-Select Unit (ACSU):** compute the state metrics
- **LLR computation unit:** compute *a-posteriori* log-likelihood ratios (LLRs) with partial maximum sharing (PMS) method [6]

warm-up sliding window

Experimental Results

- The overall VLSI implementation results.
  - DGR Design
  - MGR Design

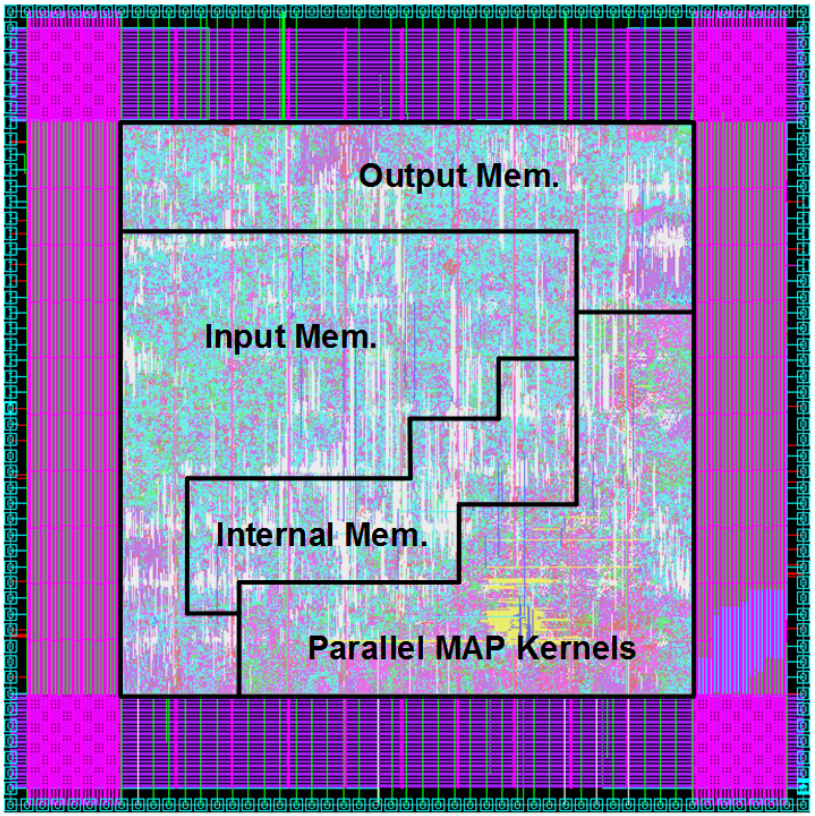




Design	Core Area (mm^2)	Global state metrics routing length (μm)
DGR	0.52	166721.1 (100%)
MGR	0.52	120465.8 (72%)

Dual-Mode TC/CC Decoder for IDD Receiver

- 第十一屆全國電子設計創意競賽 大專組電子類佳作



- 會議: **ITC-CSCC 2017 (Best Paper Award)**
- 期刊: **IEEE TCAS-I 2019**

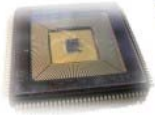
Post-layout simulation results

Technology	TSMC 40nm CMOS 1P10M
Supply Voltage	0.9 V
Core Area	2.88 mm^2
MAX. Frequency	364 MHz
Power	257 mW
	240 mW
Throughput	222 Mbps (TC)
	364 Mbps (CC)

Key Designer: Ching-Wen Hsieh (M.S. 2018)

Window-Stopped Parallel Turbo decoder for LTE Rate Matching

Department of Electrical Engineering
Yuan-Ze University, Taiwan



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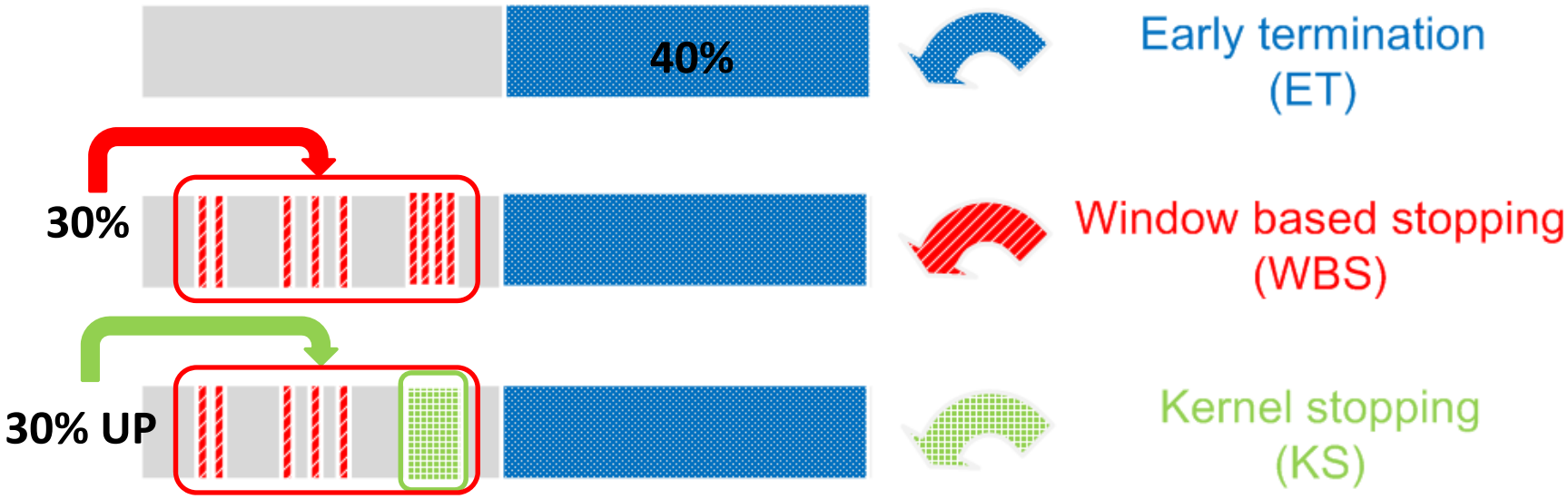
Stopping Criteria

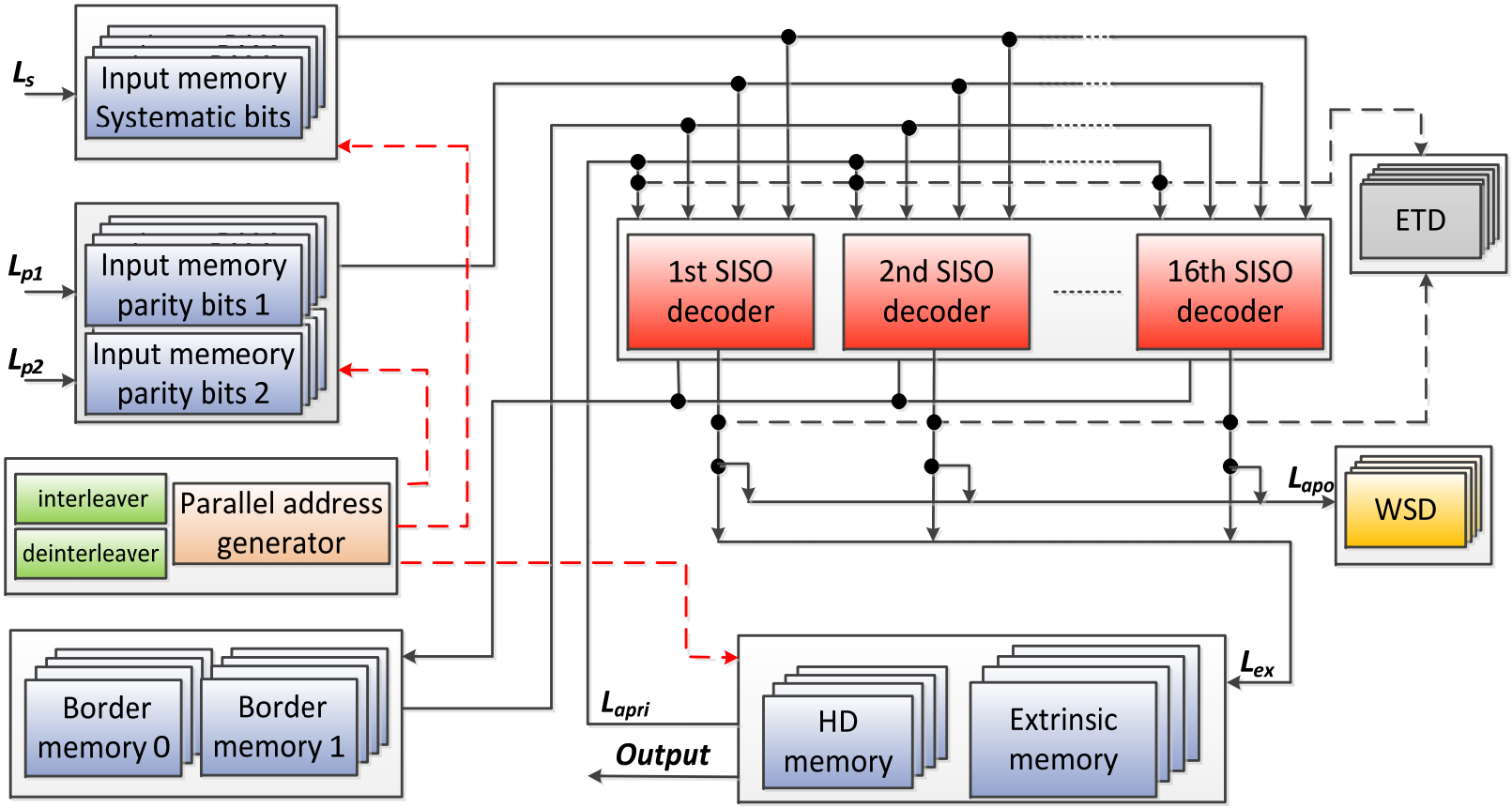
- Stopping criteria extending for turbo decoding
  - The stopping criteria have great performance on stopping rate with early termination.



[1] [2]

Proposed Decoder Architecture

- Parallel-16 turbo decoder architecture

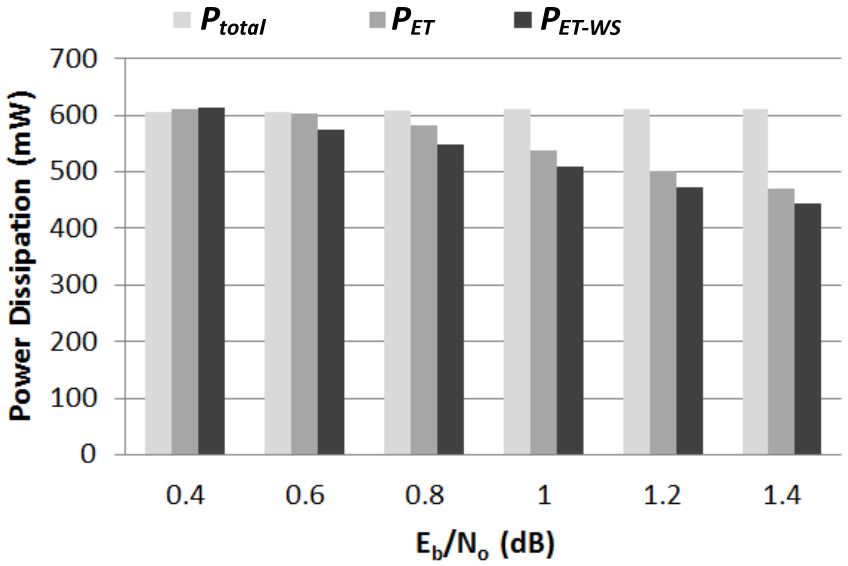


SISO : soft in soft out
HD : hard decision

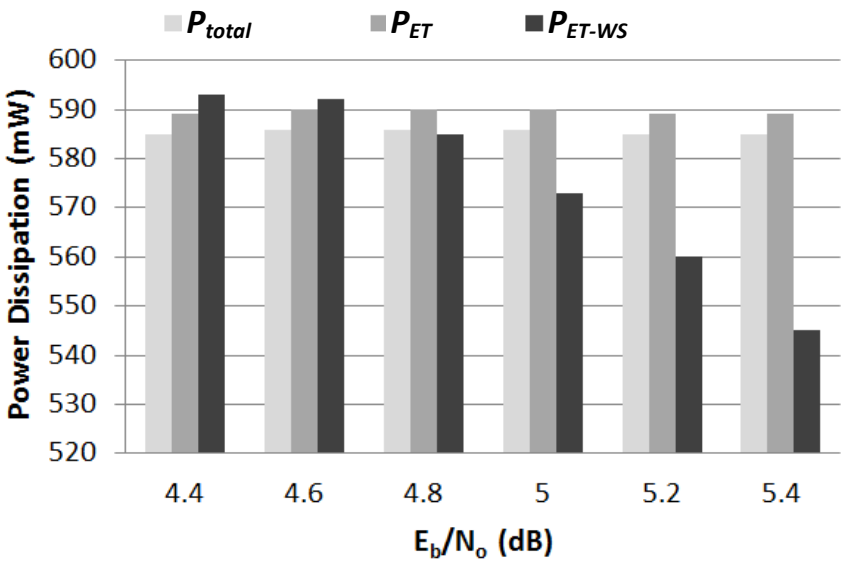
Power Dissipation for RM system

- The power dissipation of ET&WS
  - P_{ET} : Power of ET-MSDR estimation
  - $P_{ET\text{-}WS}$: P_{ET} X (1-PRR_{WS})

R = 1/3



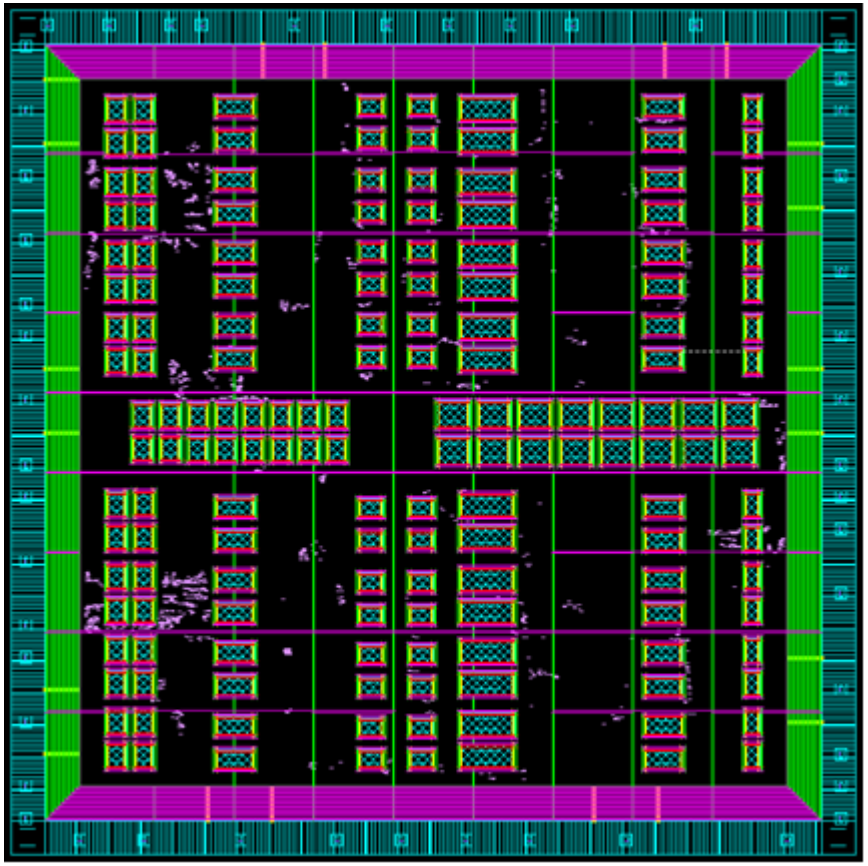
R = 0.92



Block size : 6144
Pattern : 10000
Iteration : 8

Window-Stopped Parallel Turbo Decoder for LTE Rate Matching

- 第十屆全國電子設計創意競賽大專組電子類佳作



- **Conf.: ITC-CSCC 2013**
- **Jnl.: IET COM 2018**
- **R.O.C. Patents I531171**

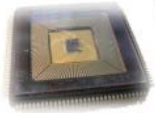
Technology	**TSMC 90nm CMOS**
Core voltage	1.0V
Core area	18.49 mm^2
Radix	Radix-2
Frequency	357 MHz
Power	614 mW
Throughput @ 6 iteration	427 Mbps

Post-layout simulation results

Key Designer: Shu-Wei Guo (M.S. 2014)

Energy-efficient LDPC Codec Design Using Cost-effective Early Termination Scheme

Department of Electrical Engineering
Yuan-Ze University, Taiwan



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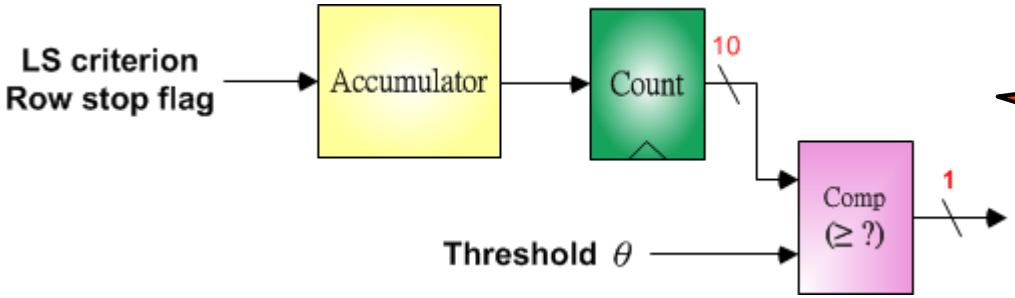
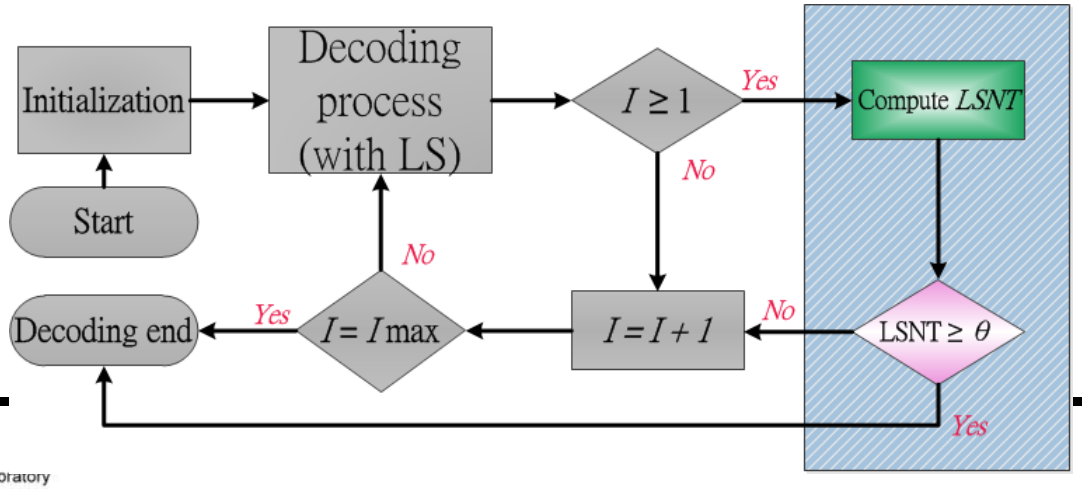
Proposed Early Termination (2/6)

- Based on the LS criterion, the layer stopping number termination (LSNT) scheme is proposed as an ET scheme.
  - **LSNT architecture**



  - **LSNT decoding flow chart**

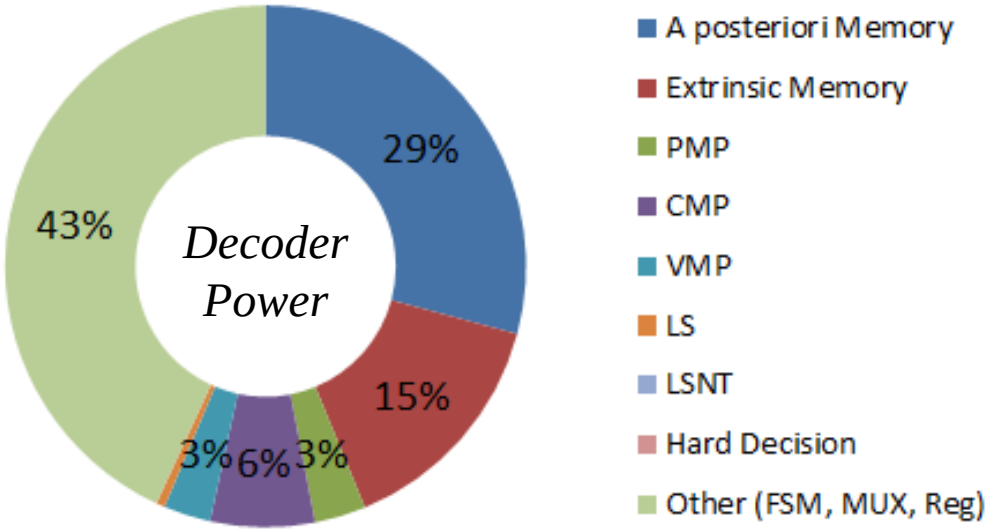


Codec Cells Area Report

NAND Flash LDPC Codec			
LDPC Encoder		**LDPC Decoder**	
Module	**Cell Area (μm^2)**	**Module**	**Cell Area (μm^2)**
XOR_group1	426	A posteriori Memory	1,671,204
XOR_group2	335	Extrinsic Memory	883,332
Others	251,918	PMP	239,055
Total encoder	(5.13%) 252,679	CMP	457,157
		VMP	245,621
		LS	(1.690%) **73,564**
		LSNT	(0.028%) **1,205**
		Hard Decision	1,705
		Other (FSM, MUX, Reg)	779,256
		Total decoder	(100%) 4,352,099
DFT cells (test coverage 99.91%)			(6.46%) 317,988
Total codec			(100%) 4,922,771

Codec Power Report

LDPC Decoder (post-DFT)	
Module	**Power (mW)**
A posteriori Memory	206.000
Extrinsic Memory	103.000
PMP	22.500
CMP	45.700
VMP	20.600
LS	(0.530%) **3.740**
LSNT	(0.014%) **0.097**
Hard Decision	0.020
Other (FSM, MUX, Reg)	304.343
Total	(100%) 706.000



Energy Consumption

- The energy consumption report during the decoding.

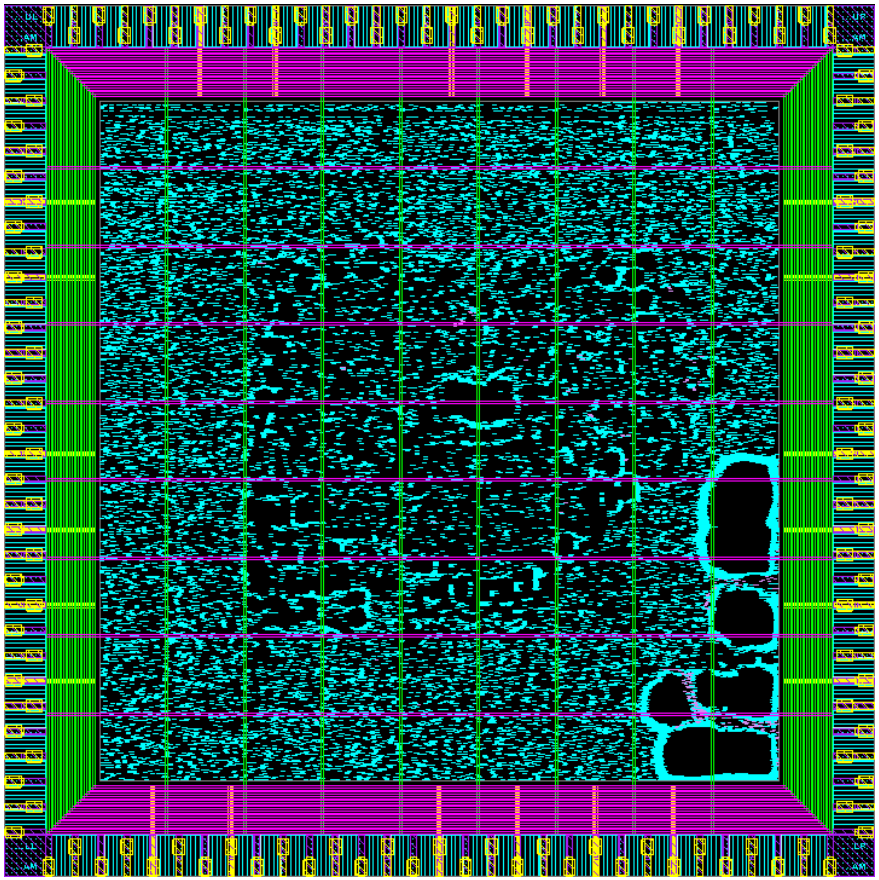
  - **Maximum iteration: 8 times**

	Energy Consumption	Ratio
Without LS and ET for 8 iteration	9.52 µJ	100 %
With LS for 8 iteration (without ET)	6.31 µJ	66.3 %
With LS and LSNT	4.32 µJ	45.4 %

Energy consumption  

Energy-efficient LDPC Codec for Non-Volatile Memories

第十二屆全國電子設計創意競賽大專組
電子類佳作



- **Conf.: IEEE GCCE 2014**
- **Jnl.: IET CDT 2019**

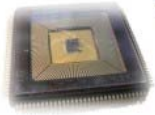
Post-layout simulation results

Cell Library	TSMC 90nm Process
Work Voltage	1.0V/3.3V
Applications	NAND Flash ECC
Codeword Size	8,960
Code Rate	0.91
Core Size	9.86 mm^2
Work Frequency	278 MHz
Power Consumption	968 mW
Throughput for Encoder	4448 Mbps
Throughput for Decoder	4313 Mbps

Key Designer: Yuan-Syun Wu (M.S. 2015)

Multi-Mode SISO Kernel Using Unified Encoder Embedded Trellis Router

Department of Electrical Engineering
Yuan-Ze University, Taiwan



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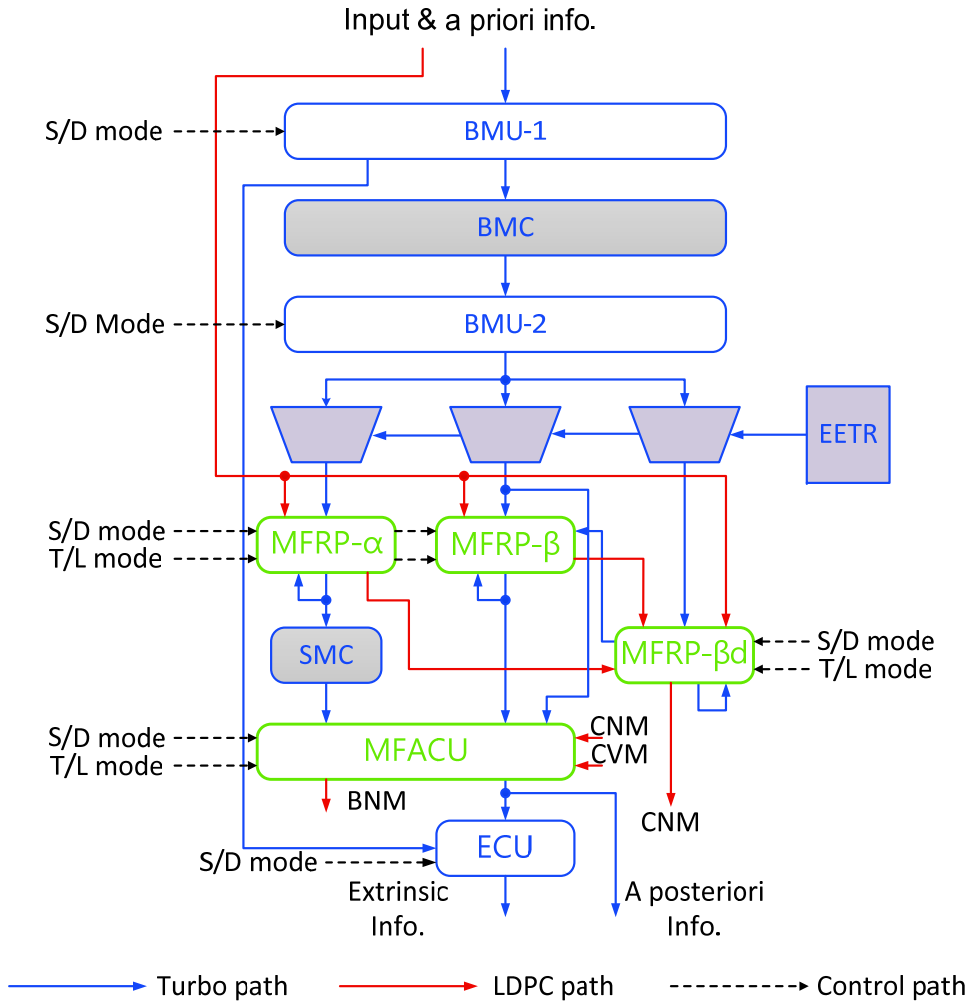
Multi-Mode SISO Kernel with EETR

- The MSISO with R-4UEETR.
- Able to decode CC, SB/DBTC and LDPC with decoding latency at 8 cycles.



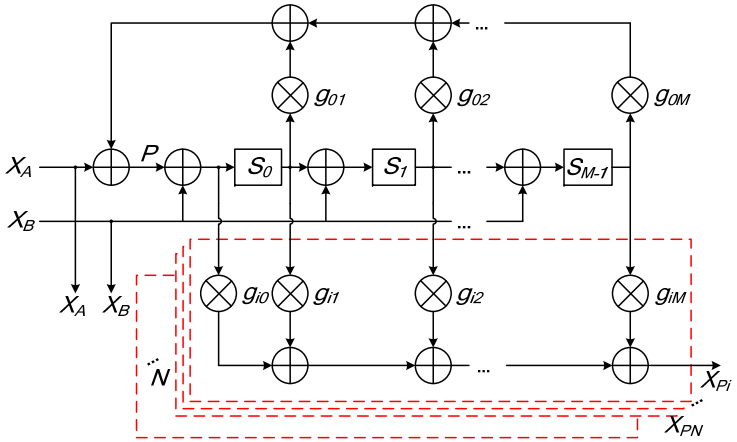
BMU: Branch Metric Unit
BMC: Branch Metric Cache
MFRP: Multi Function Recursive Processing
MFACU: Multi Function a posteriori Calculation Unit
SMC: State Metric Cache
ECU: Extrinsic Calculator Unit
EETR: Encoder Embedded Trellis Router

Double Binary Radix-4 EETR

- To generate the path, extend the application range as well, EETR is extended into both radix-4 and DBTCs.

For a DB RSC encoder:

$$\begin{cases} X_A = P \oplus (g_{01} \cdot S_0) \oplus (g_{02} \cdot S_1) \oplus \cdots \oplus (g_{0M} \cdot S_{M-1}), \\ X_{Pi} = X_B \oplus (g_{i0} \cdot P) \oplus (g_{i1} \cdot S_0) \oplus \cdots \oplus (g_{iM} \cdot S_{M-1}). \end{cases}$$

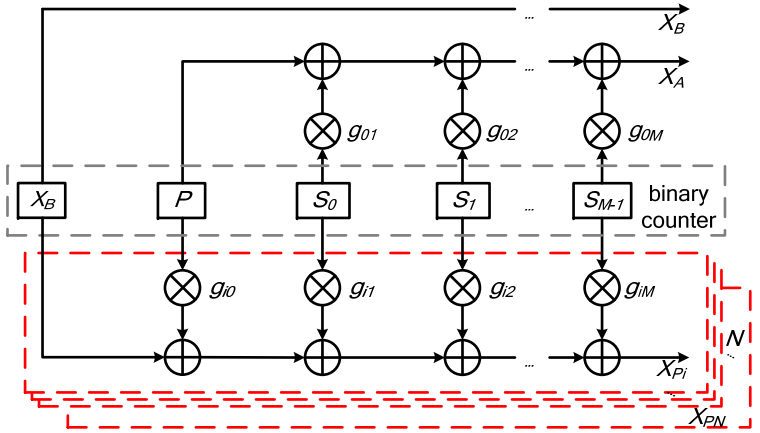


For SBTCs:

$$\begin{cases} X_{S,0} = P_1 \oplus (g_{01} \cdot S_0) \oplus (g_{02} \cdot S_1) \oplus (g_{03} \cdot S_2), \\ X_{S,1} = P_0 \oplus (g_{01} \cdot P_1) \oplus (g_{02} \cdot S_0) \oplus (g_{03} \cdot S_1), \\ X_{Y,0} = (g_{10} \cdot P_1) \oplus (g_{11} \cdot S_0) \oplus (g_{12} \cdot S_1) \oplus (g_{13} \cdot S_2), \\ X_{Y,1} = (g_{10} \cdot P_0) \oplus (g_{11} \cdot P_{k-1}) \oplus (g_{12} \cdot S_0) \oplus (g_{13} \cdot S_1). \end{cases}$$

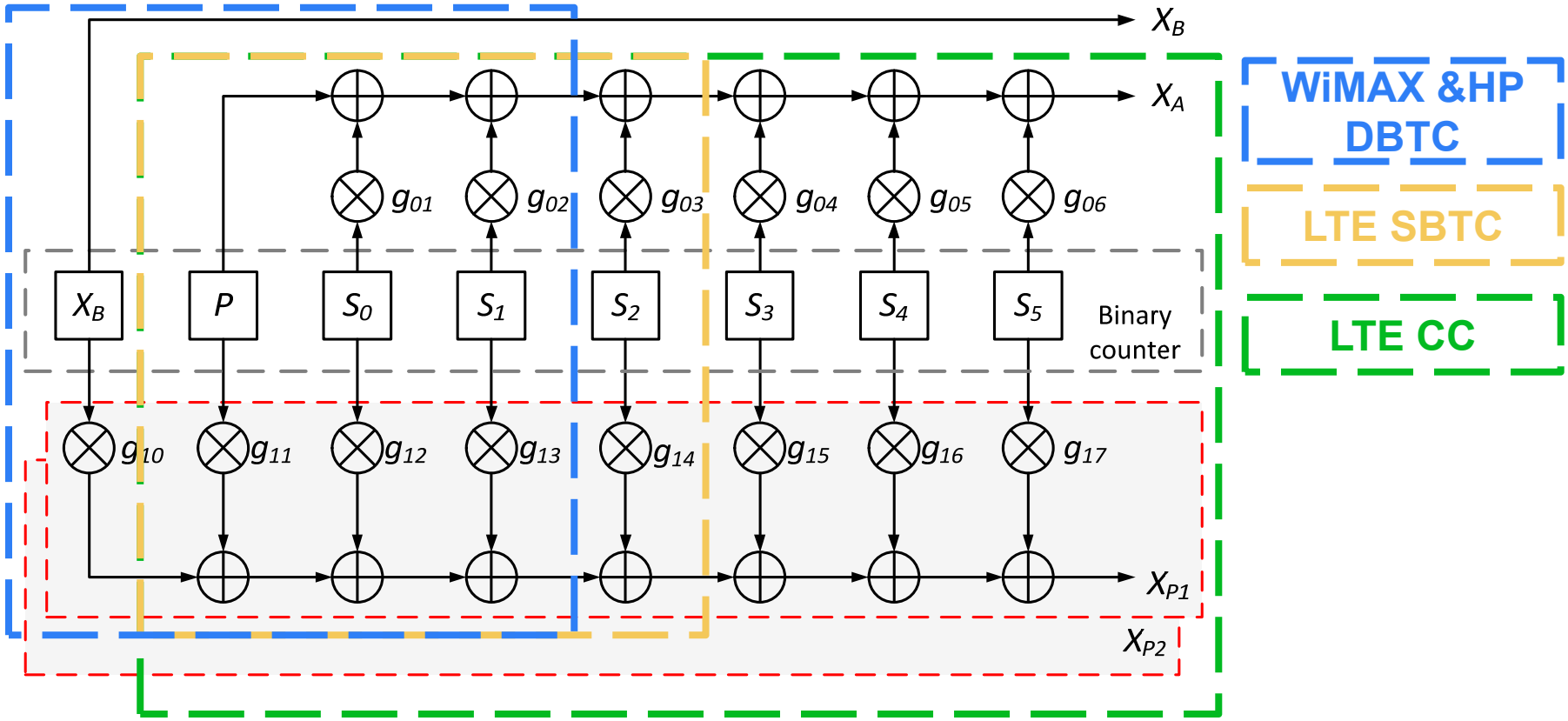
For DBTCs:

$$\begin{cases} X_A = P_1 \oplus (g_{01} \cdot S_0) \oplus (g_{02} \cdot S_1) \oplus (g_{03} \cdot S_2), \\ X_B = P_0, \\ X_{P1} = P_0 \oplus (g_{10} \cdot P_1) \oplus (g_{11} \cdot S_0) \oplus (g_{12} \cdot S_1) \oplus (g_{13} \cdot S_2), \\ X_{P2} = P_0 \oplus (g_{20} \cdot P_{10}) \oplus (g_{21} \cdot S_0) \oplus (g_{22} \cdot S_1) \oplus (g_{23} \cdot S_2). \end{cases}$$



Double Binary Radix-4 EETR (4/4)

- EETR for TCs and CC in WiMAX, LTE.



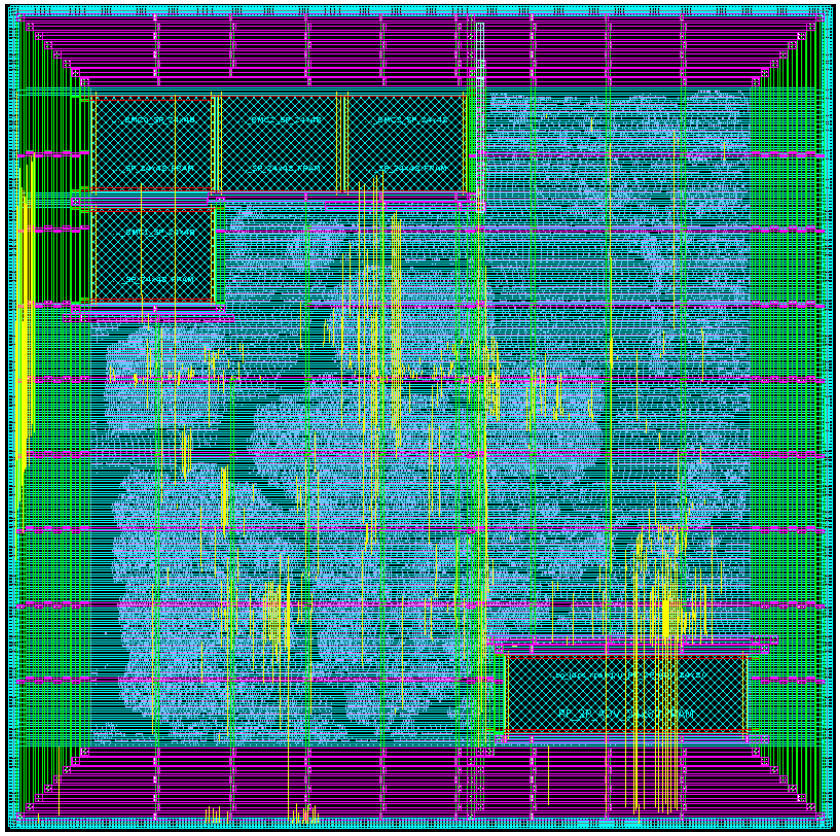
Experimental Results

- Synthesis results with TSMC 90 nm technology @240 MHz

Module	Area (Occupation)	
BMU	9384.43	13.1%
Recursive - $\alpha + \beta + \beta_d$	53506.02	74.5%
ACU	29168.79	40.6%
ECU	2824.51	1.1%
BMC	53583.06	20.9%
SMC	27532.6	10.8%
Controller + Path Mux. + Pipeline Reg.	71833.91	28.1%
EETR	8162.31	3.2%
Overall	255995.63	100.0%

Multi-Mode SISO Kernel Using UEETR (1/2)

- 第十屆全國電子設計創意競賽
大專組電子類佳作



- **Jnl.: IEICE EXEL 2017**
- **R.O.C. Patent I599182**
- **U.S. Patent 9,787,331 B1**

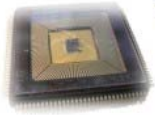
Technology	TSMC 90nm CMOS		
Core Voltage	1.0V		
Core Size	0.48 mm^2		
Radix-r	Radix-4		
Code Type	SB CC	SB/DB TC	LDPC
Decoding Strategy	SW	SW	TPMP
Decoding Algorithm	EML-MAP	EML-MAP	FBA
MAX. Frequency	166.7 MHz		
Throughput (@8 iter.)	333 Mbps	333 Mbps	800 Mbps

Post-layout simulation results

Key Designer: Tsung-Ju Hsieh (M.S. 2016)

Operation-Reduced LDPC Decoder Using a Check Node Stopping Scheme

Department of Electrical Engineering
Yuan-Ze University, Taiwan



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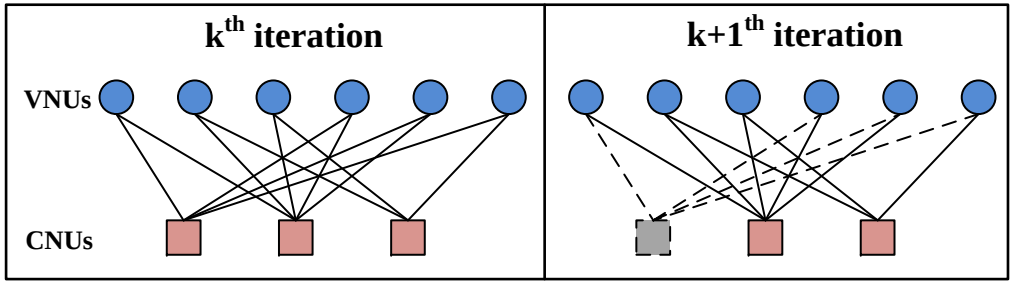
Check Node Stopping Criterion

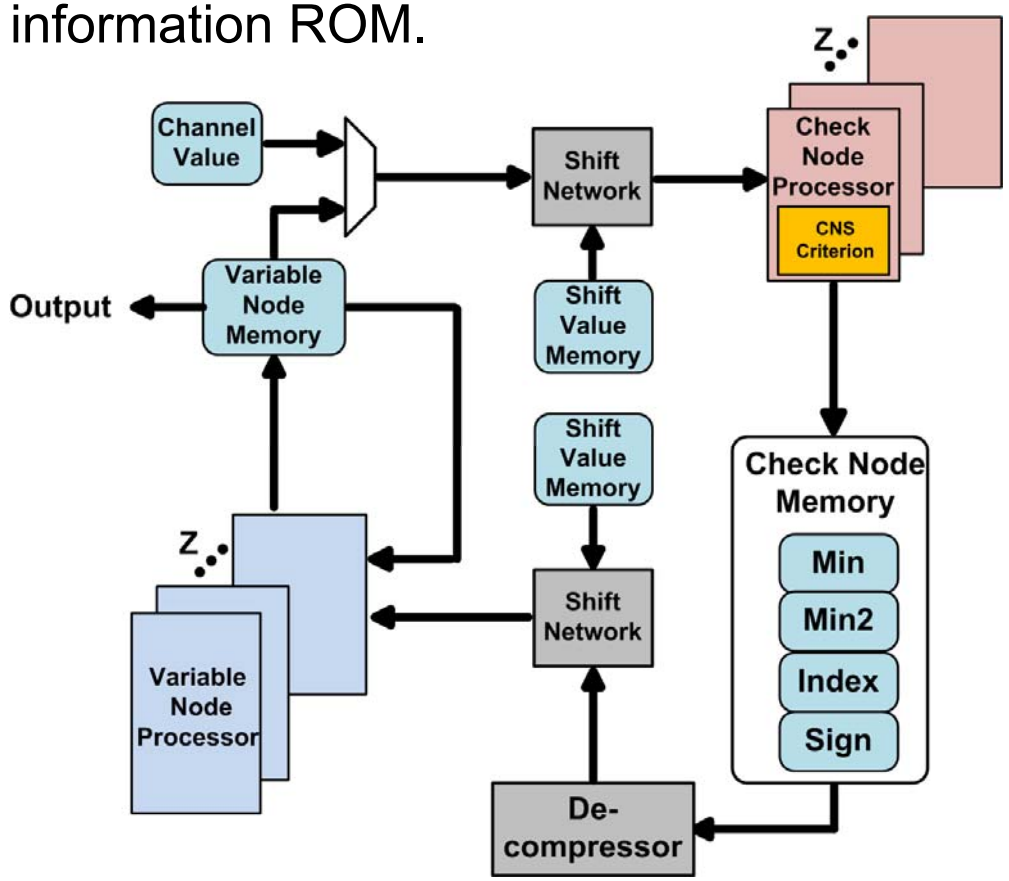
- Check node units and memory operate state with node stopping criterion.



	Non-convergent Node	Convergent Check Node
Variable Node Operation	ON	ON
Check Node Operation	ON	OFF
LLR	ON	ON
Variable Node Memory Access	ON	ON
Check Node Memory Access	ON	OFF

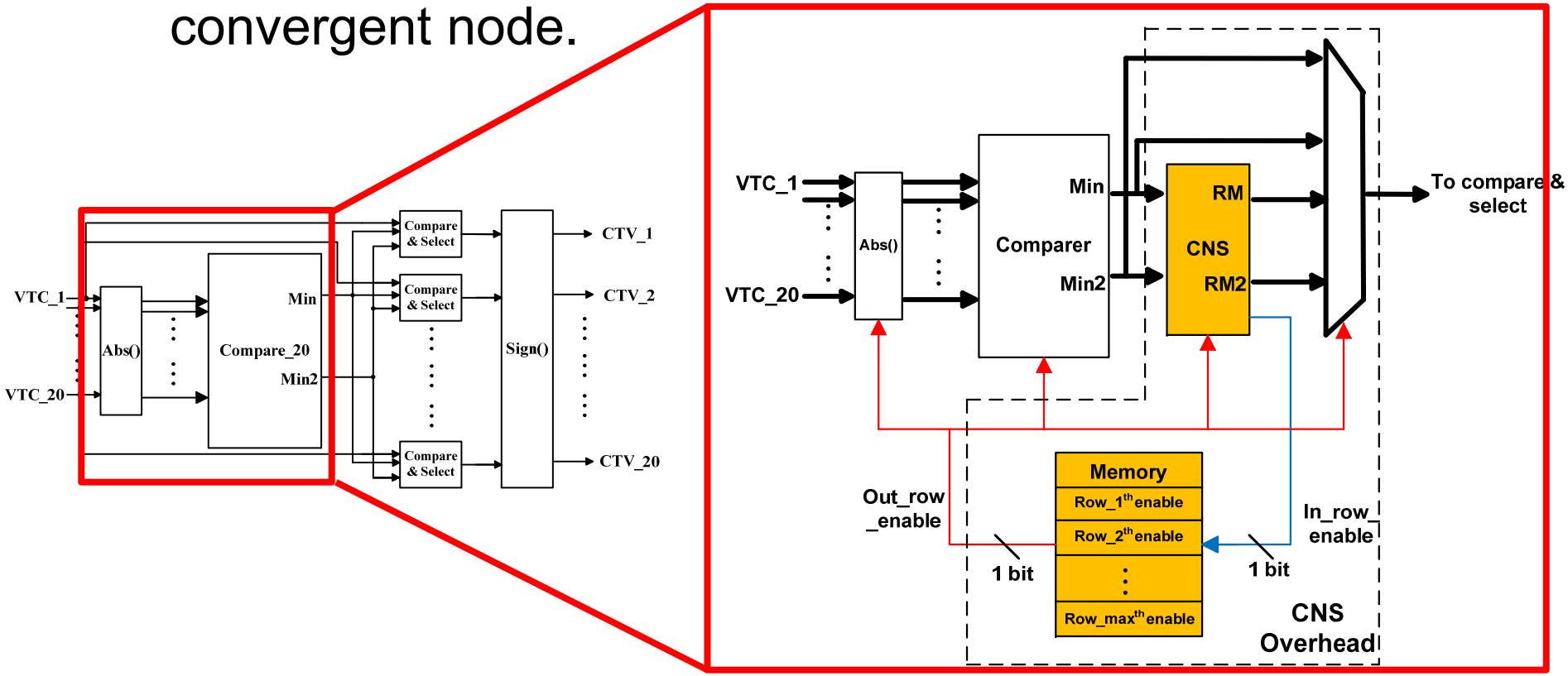
VLSI Design of LDPC Decoder

- The proposed LDPC decoder consists of check node units, variable node units, a variable node memory, a check node memory, channel value memory, shift network, and parity check matrix *H* information ROM.



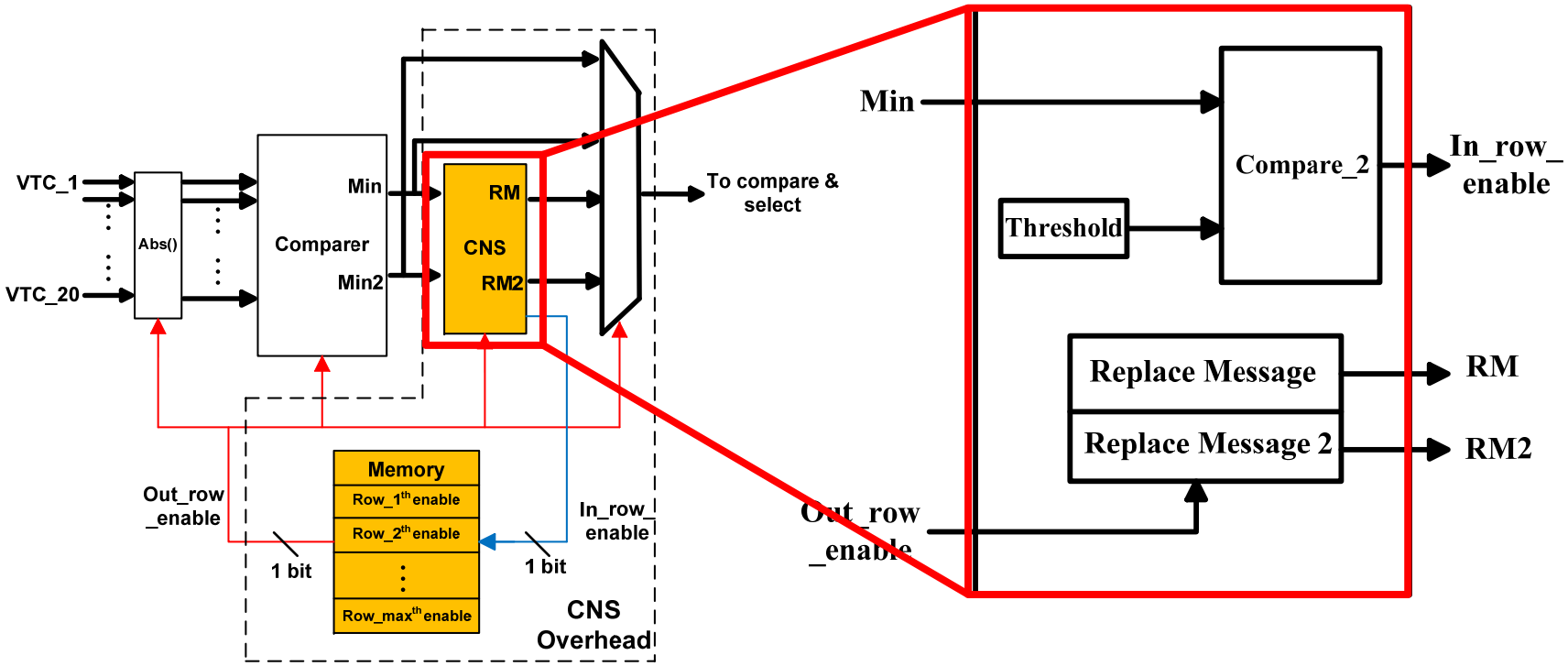
CNU Design (1/2)

- The CNS checks whether the absolute values of the check node message larger than the threshold or not.
- The memory store which enable address of the convergent node.



CNU Design (2/2)

- The CNS checks whether the absolute values of the check node message larger than the threshold.
- When the absolute values of check node message are larger than threshold, CNS sends RM and RM2 to replace the Min and Min2.



Experimental Results

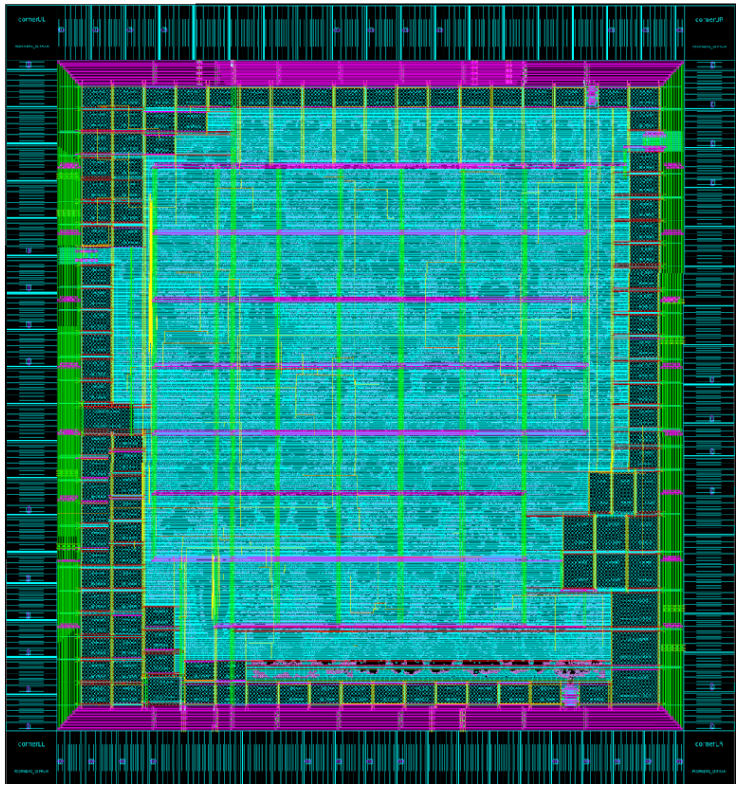
- The power comparison between non-convergent node and convergent node.

	Original LDPC Decoder (mW)	Proposed LDPC Decoder	
		Non-Convergent Node (mW)&	Convergent Node (mW)&
Variable Node Operation	8.3	8.3	8.3
Check Node Operation	33.1	33.1	28.1
Variable Node Memory Access	9.4	9.4	9.4
Check Node Memory Access	10.2	10.2	8.6
Shift network	43.7	43.7	43.7
Channel Memory Access	4.7	4.7	4.7
CNS	N/A	1.1	1.1
Total	109.4 (100%)	110.5 (101%)	104.0 (95%)

& at Eb/N0 = 3.6, Threshold = 13

Operation-Reduced LDPC Decoder for WiMAX Standard

- 第十屆全國電子設計創意競賽大專組電子類佳作



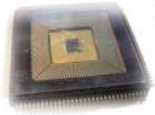
- Conf.: IEEE ISCE 2014, ITC-CSCC 2013
- Jnl.: JCSC 2017

Cell Library	TSMC 90 nm CMOS
Work Voltage	1.0V/3.3V
Gate Count	672K
Code Size	2.1mm × 2.1mm
Die Size	2.7mm × 2.7mm
Operating Frequency	100MHz
Maximum Throughput Rate @8 iter.	226.8 Mbps
Power Consumption	106.2mW

Post-layout simulation results

Layer-Stopped LDPC Decoder for DSRC Systems

Department of Electrical Engineering
Yuan-Ze University, Taiwan



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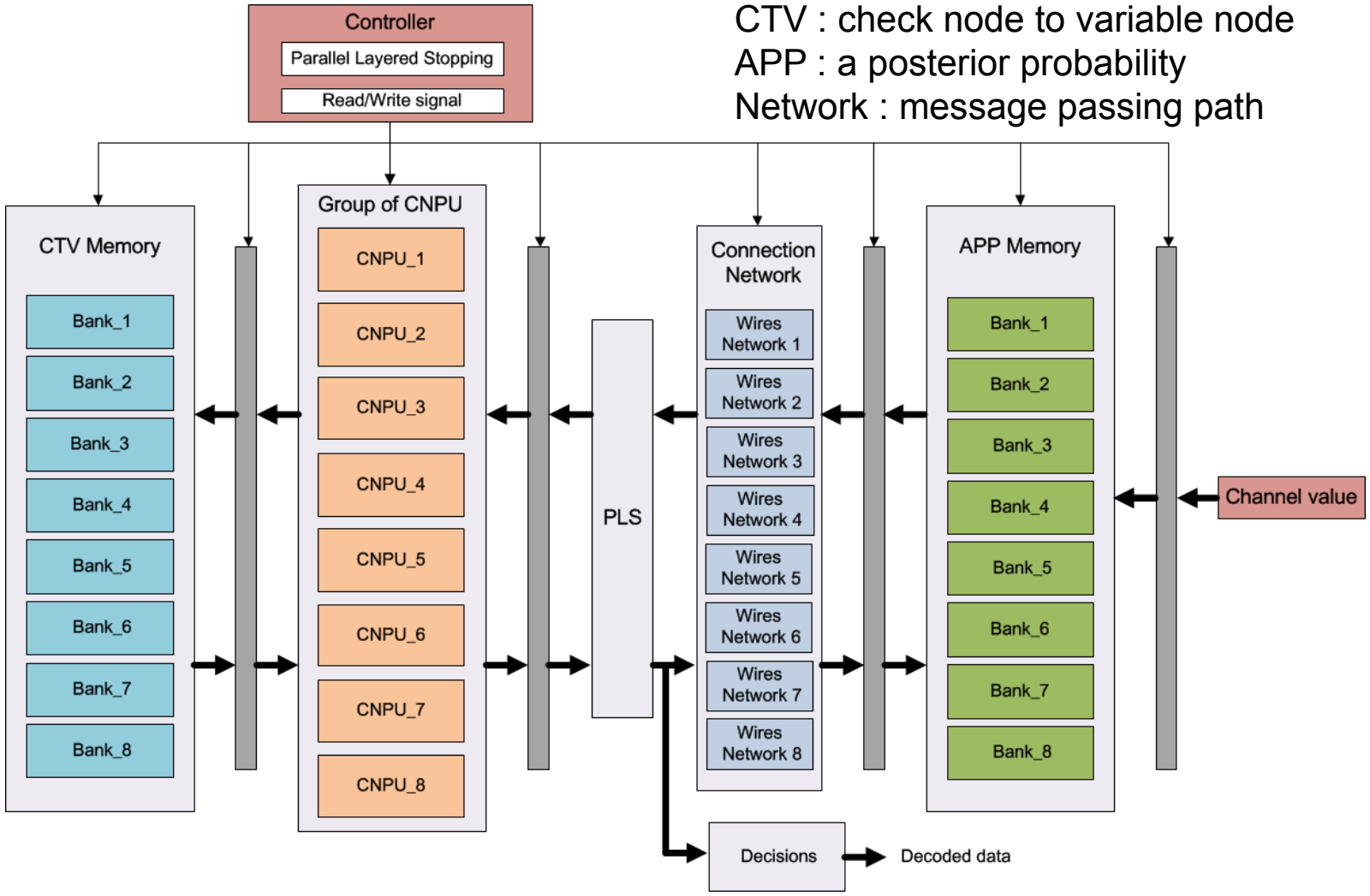
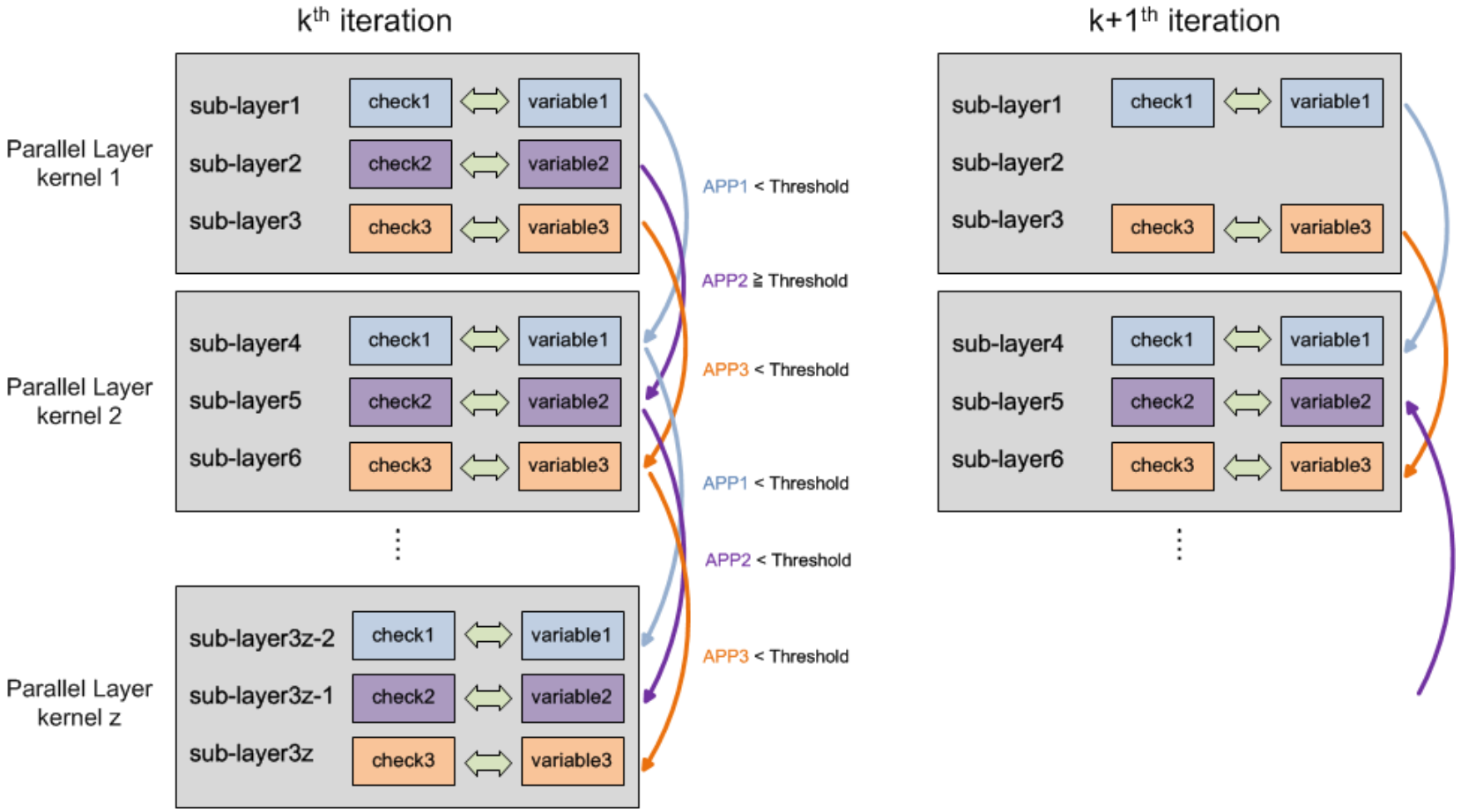
Layer-Stopped LDPC Decoder for DSRC Systems

CNPU : check node processing unit
CTV : check node to variable node
APP : a posterior probability
Network : message passing path



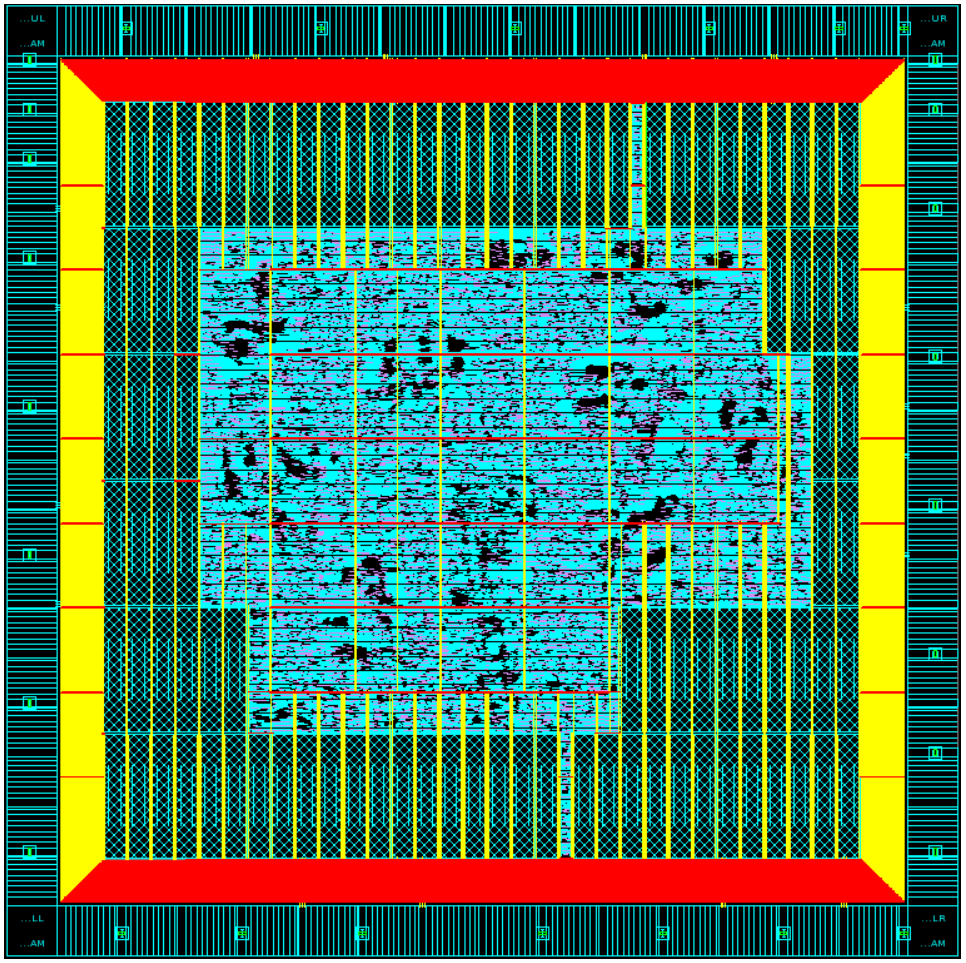
Parallel Layered Stopping

- Assuming APP2 $\geqq$ threshold in Parallel Layer kernel 1 in current iteration, we will stop it in the following iterations.



Layer-Stopped LDPC Decoder for DSRC Systems

2018年台灣創新技術博覽會發明競賽銀牌獎



- **Conf.: ITC-CSCC 2013**
- **Jnl.: IET EL 2013**
- **R.O.C. Patent I504162**
- **U.S. Patent 9,344,116 B2**

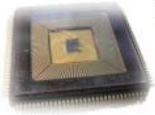
Post-layout simulation results

Cell Library	TSMC 0.18μm
Work Voltage	1.8V
Gate Count	843K
Core Size	2.9mm×2.9mm
Die Size	3.3mm×3.3mm
Operating Frequency	250 MHz
Power Consumption (Block length = 2048) (Iteration = 16)	212mW@2.5dB (w/o PLS) 162mW@2.5dB (w/ PLS)

Key Designer: Shin-An Chou (M.S. 2012) & Tzu-Hsuan Huang (M.S. 2012)

Multi-mode Radix-4 Turbo/LDPC Decoding Kernel

Department of Electrical Engineering
Yuan-Ze University, Taiwan



VSPS Lab.
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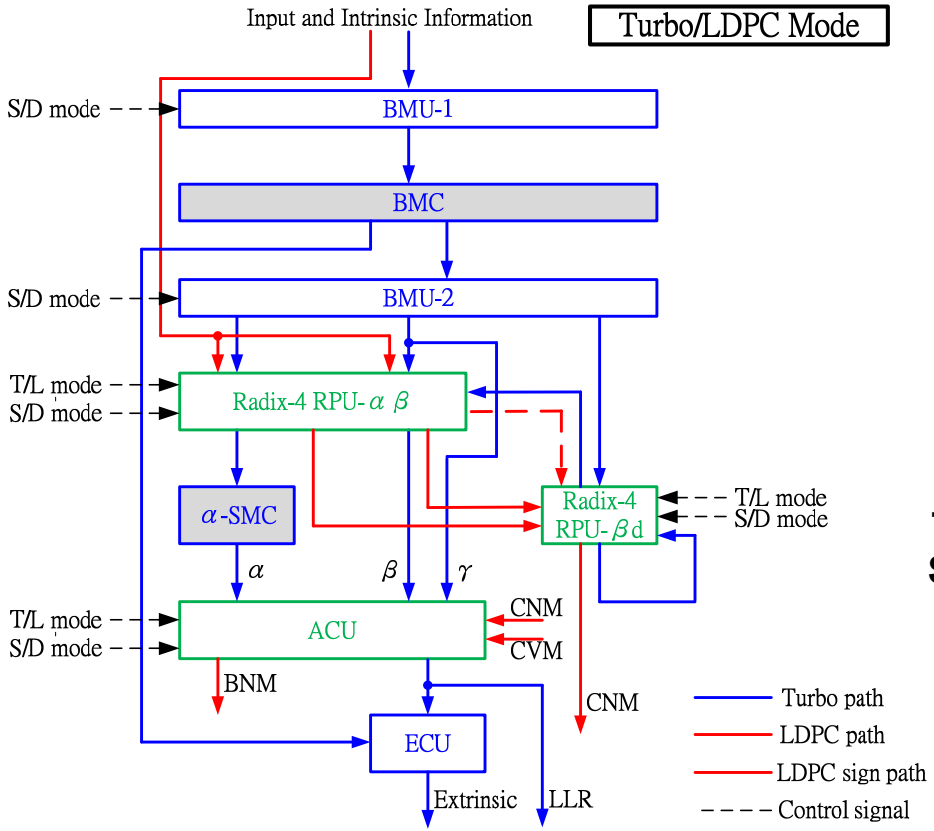
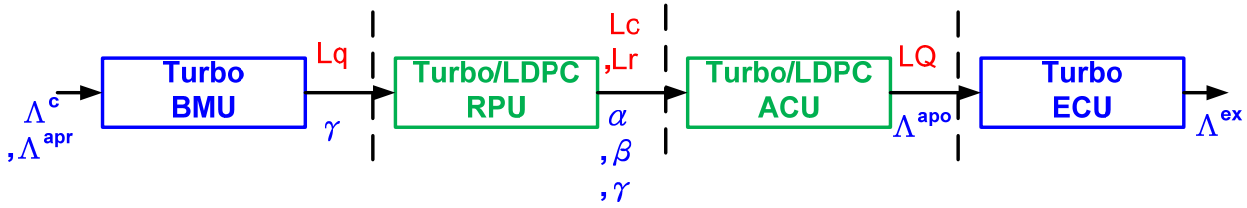
Multi-mode Radix-4 Turbo/LDPC Decoding Kernel



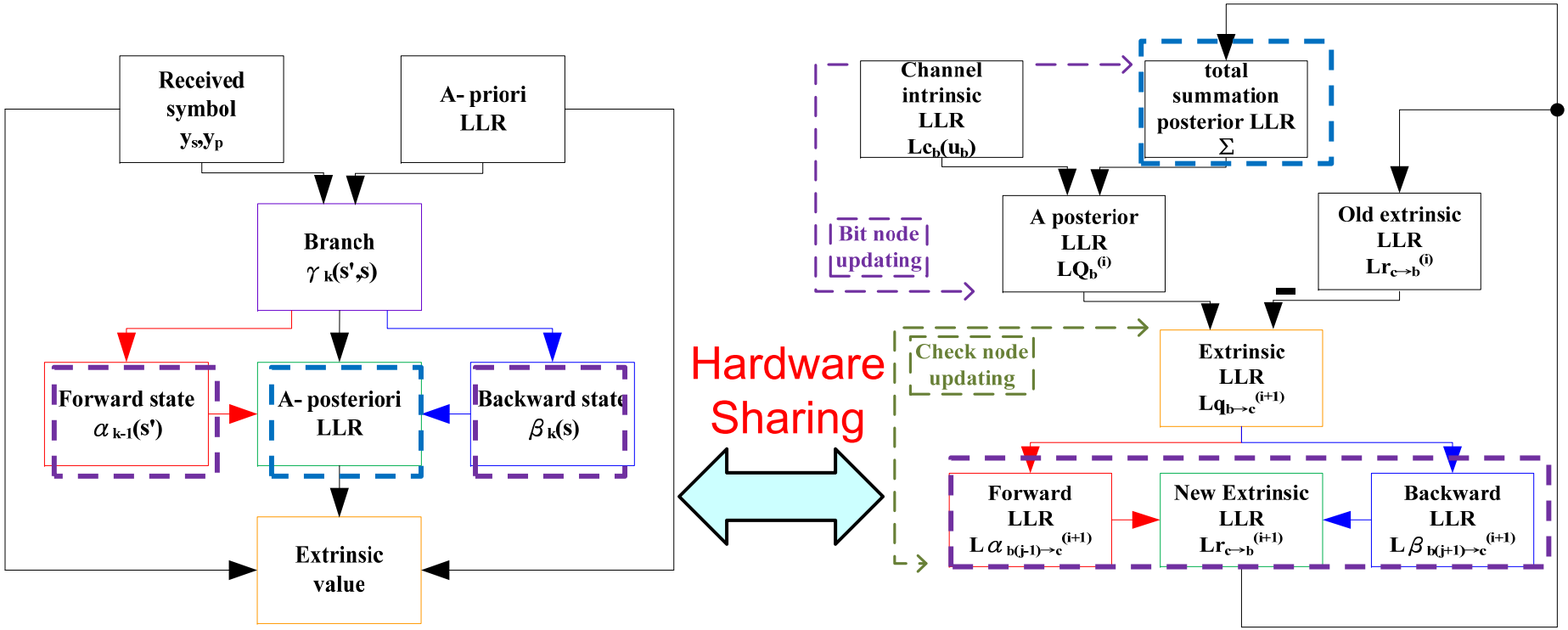
BMU:	Branch Metrics Calculator
BMC:	Branch Metrics Cache
RPU-αβ:	Recursion Processor Unit - Alpha Beta
RPU-β_d:	Recursion Processor Unit- Dummy Beta
α-SMC:	Alpha-Sate Metrics Cache
ACU:	A-posteriori Calculator Unit
ECU:	Extrinsic Calculator Unit
CNM:	Check Node Memory
BNM:	Bit Node Memory
CVM:	Channel Value Memory
T/L mode:	Turbo/LDPC Mode
S/D mode:	Single/Double Mode

Operating mode:
(1) Radix-4 SB EML-MAP decoding
(2) Radix-4 DB EML-MAP decoding
(3) Radix-4 FBA decoding



Combination of Radix-4 MAP and FBA

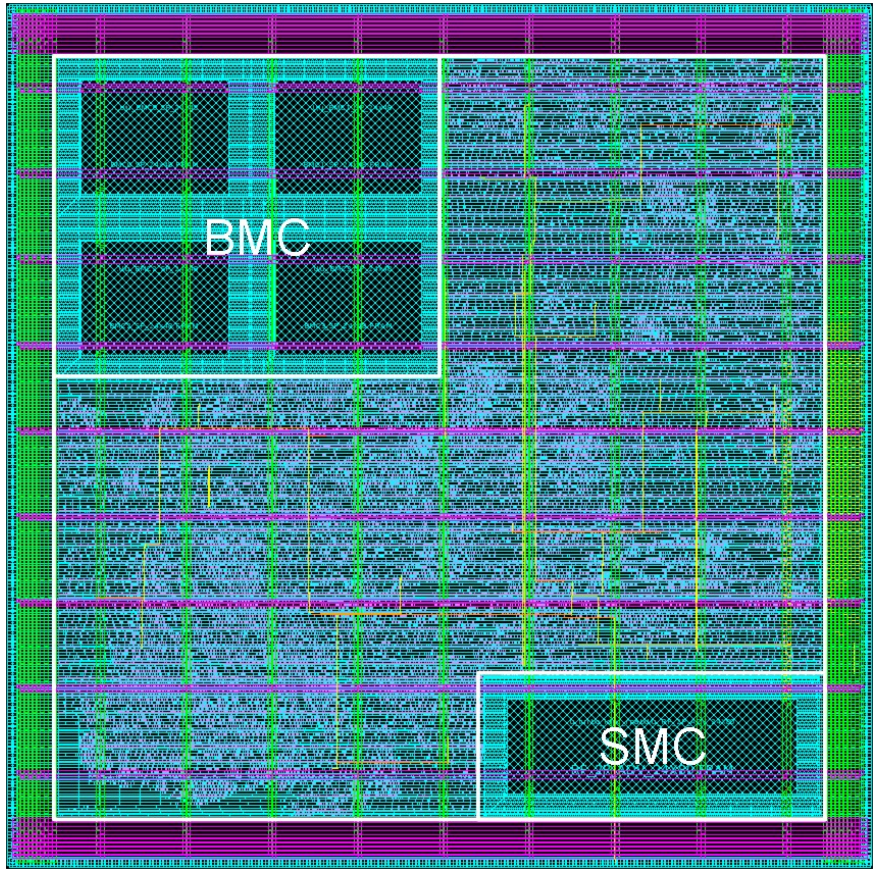
- Radix-4 MAP for DB/SBTC
- Radix-4 FBA for LDPC



- Proposed combination of radix-4 MAP and radix-4 FBA.
- The MAP equations have similar computations to FBA equations
  - They have many commonalities favorable for implantation.

Multi-mode Radix-4 Turbo/LDPC Decoding Kernel

- 會議: ITC-CSCC 2012
- 期刊: IEEE TVLSI 2015



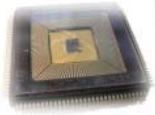
Post-layout simulation results

Technology	TSMC 90 CMOS	
Decoding Algorithm	*T:*	DB/SB EML-MAP
	L:	Radix-4 FBA
Decoding Strategy	*T:*	Hybrid Window
	L:	Two-Phase
Supply Voltage	1.0 V	
MAX. Frequency	167 MHz	
Core Size	0.67×0.67 mm^2	
Throughput Rates	*T:*	333 Mbps
	L:	800 Mbps
Power	*T:*	169.8 mW
	L:	36.1 mW

Key Designer: Chih-Shiang Yu (M.S. 2013)

Window-Based Stopping Turbo Decoder for WiMAX Standard

Department of Electrical Engineering
Yuan-Ze University, Taiwan



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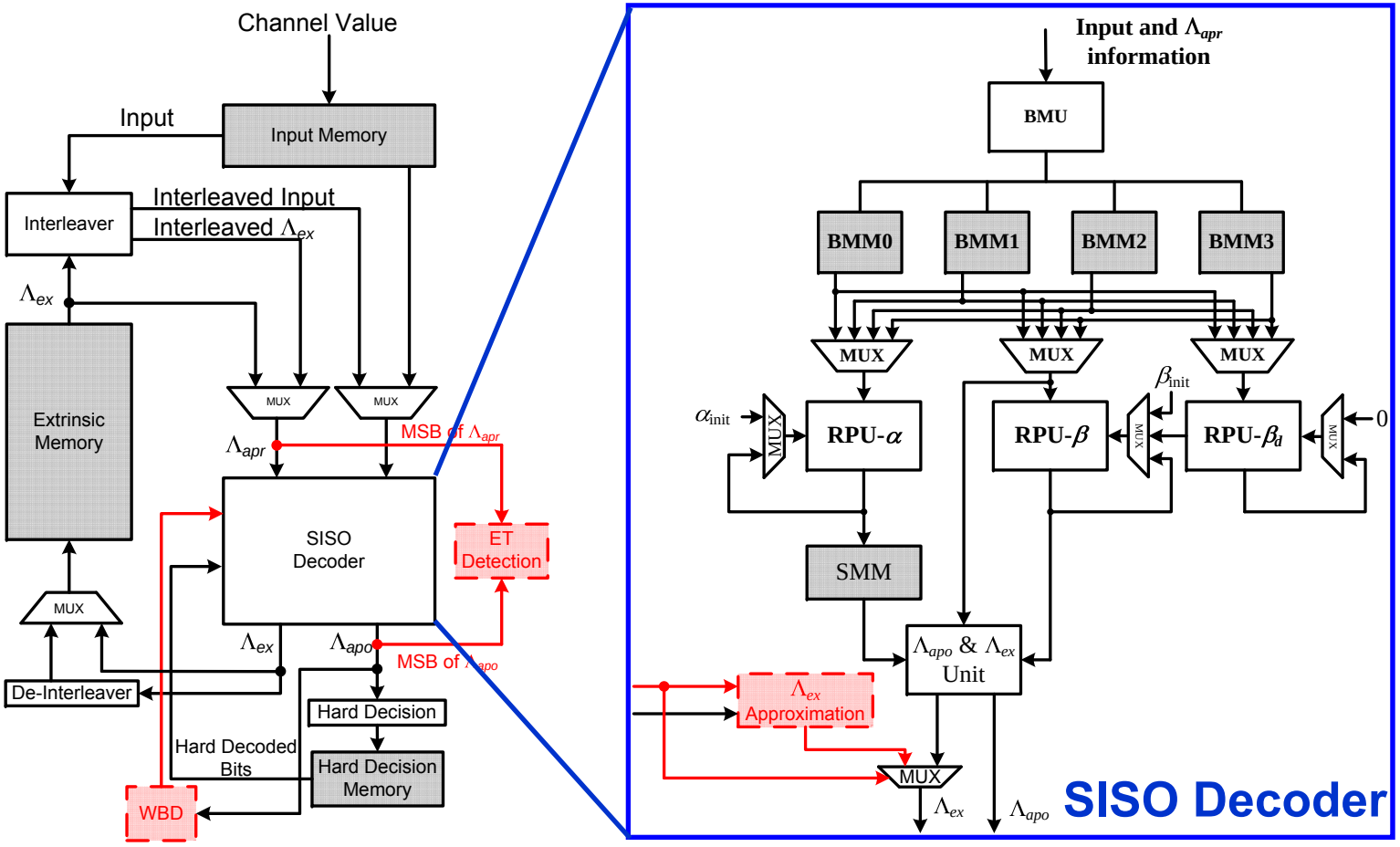
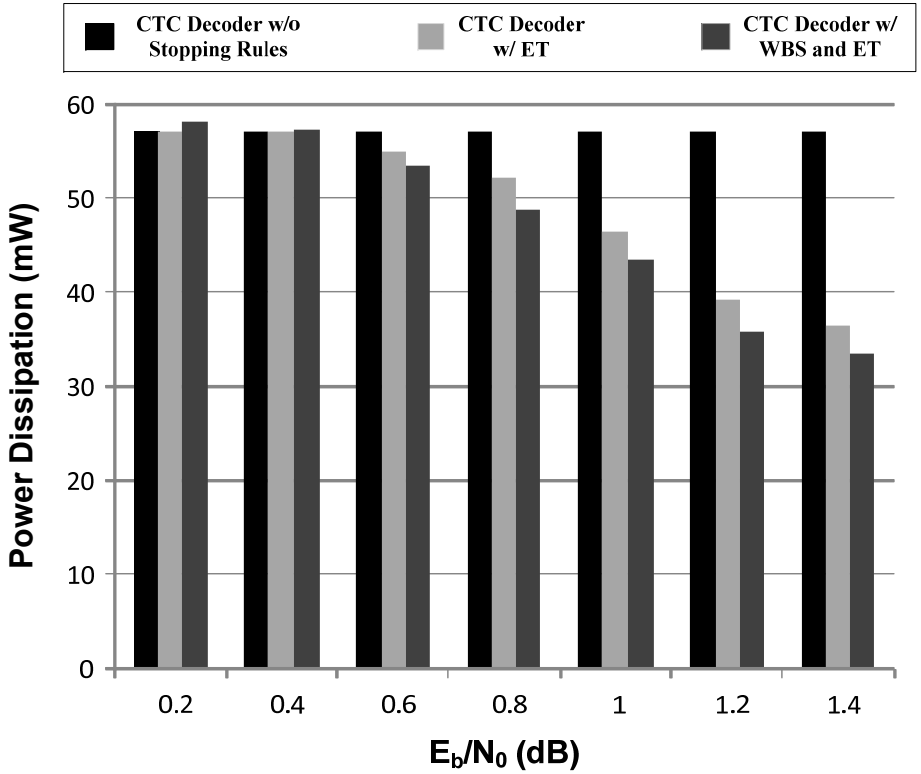
Window-Based Stopping Turbo Decoder for WiMAX Standard

- The block diagram of proposed CTC decoder
- The blocks with dashed line are for implementation overhead.



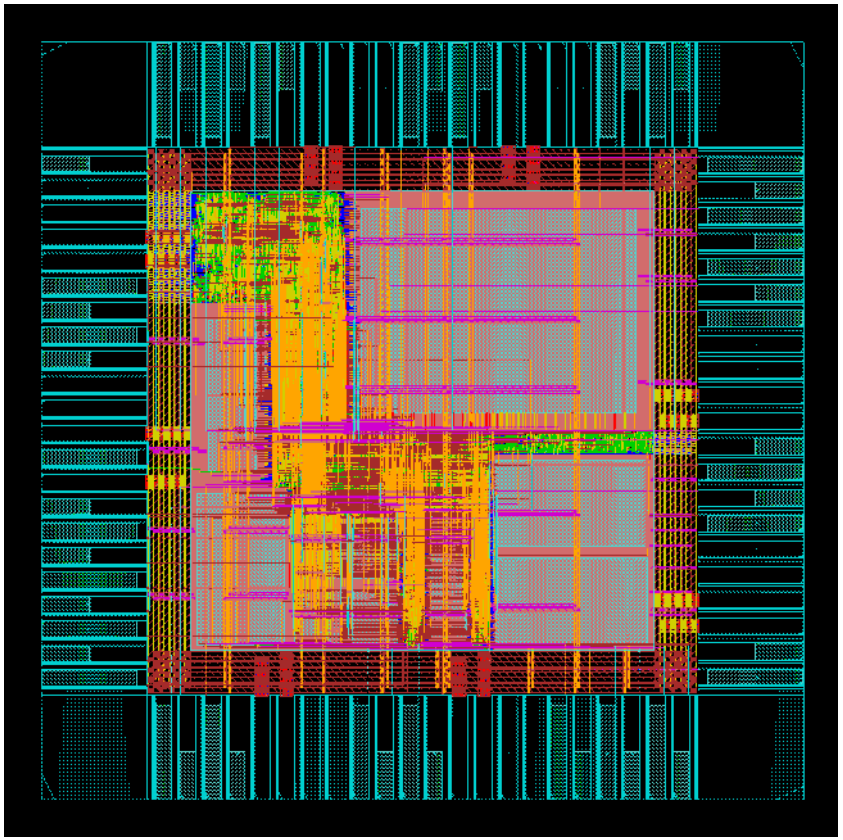
Power Evaluation of Proposed CTC Decoder

- The power dissipation of proposed CTC decoder (including the power dissipation of external memory).



- **Above E_b/N_0 0.8 dB**
- **About 14%~41% power reduction compared with CTC decoder w/o stopping rules.**
- **About 6%~9% power reduction compared with CTC decoder w/ ET.**

Window-Based Stopping Turbo Decoder for WiMAX Standard



- **Conf.: ITC-CSCC 2012, IEEE APC-CAS 2012**
- **Jnl.: IEEE Commun. Lett. 2013**
- **R.O.C. Patents I531171**

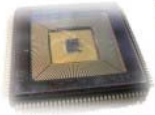
Post-layout simulation results

Technology	**TSMC 90 nm CMOS**
Decoding Algorithm	**EML-MAP**
Decoding Type	**Radix-4 DB**
Window Type	**SW**
Supply Voltage	**1.0 V/3.3 V**
Max. Frequency	**250 MHz**
Core Size	**0.83×0.83 mm^2**
Max. Throughput Rates @ 8 iter.	**30.2 Mbps**
Maximum Power	**58.1 mW**

Key Designer: Chih-Chia Wei (M.S. 2012)

Prof. C.-H. Lin's Previous Works

Department of Electrical Engineering
Yuan-Ze University, Taiwan



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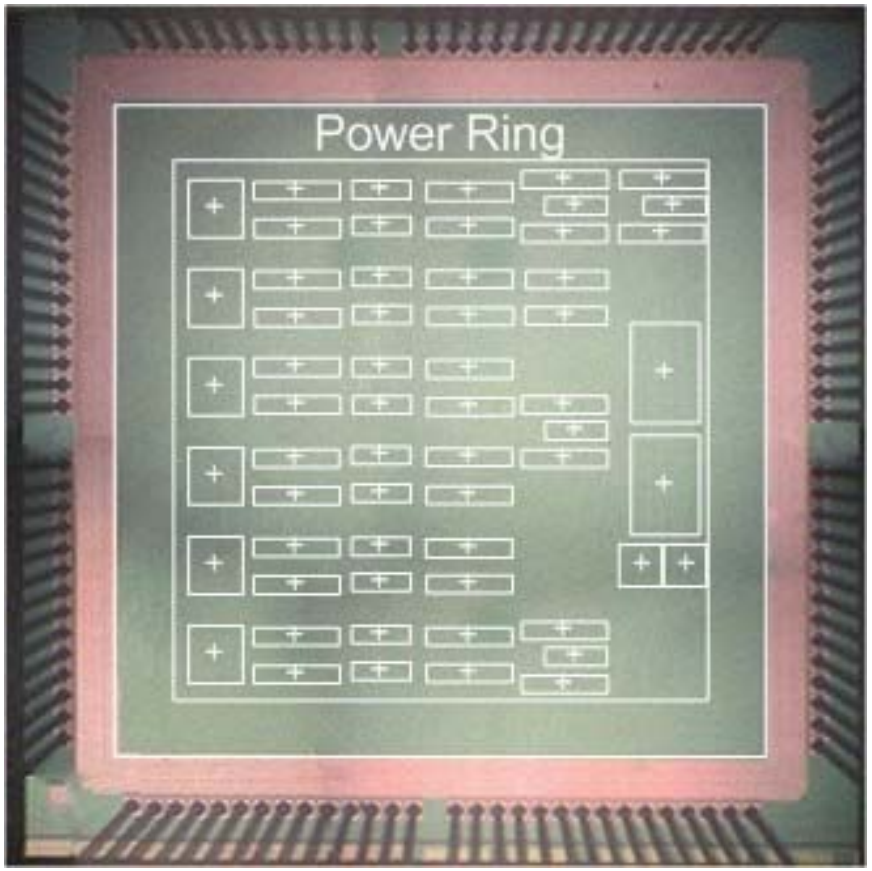
35-Mode LTE/WiMAX CTC Decoder

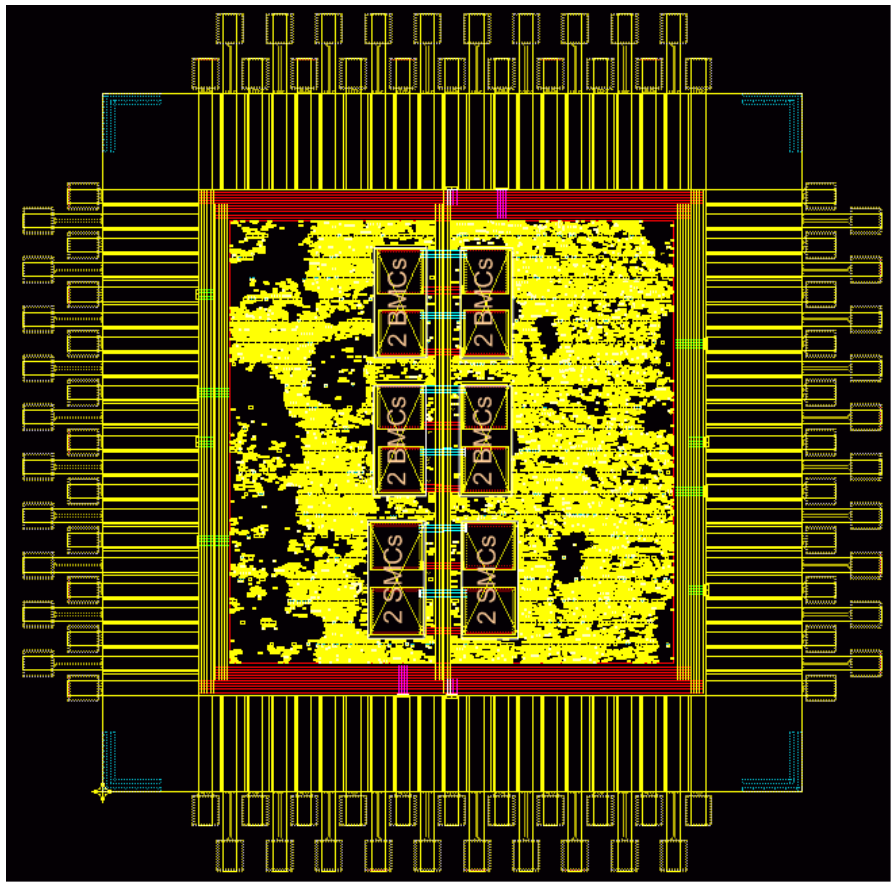


- 會議: **ISIC 2012**
- 期刊: **JSPS 2013**
- **2010**國家晶片系統設計中心晶片製作 優良設計獎
- 第九屆旺宏金矽獎-設計組 銅獎

Measurement results

Technology	UMC 90nm 1P9M
Supply Voltage	1.1 V/4.5 V
Core Size	1.84 x 1.83 mm^2 (3.38 mm^2)
Decoding Algorithm	EML-MAP
Max. Frequency	152 MHz
Throughput Rates @5 Iterations	186.1 Mbps (LTE, N = 6144)
	178.4 Mbps (WiMAX , N = 4800)
Power	148.1 mW (LTE, N = 6144)

2PW-1HW MAP Processor Chip

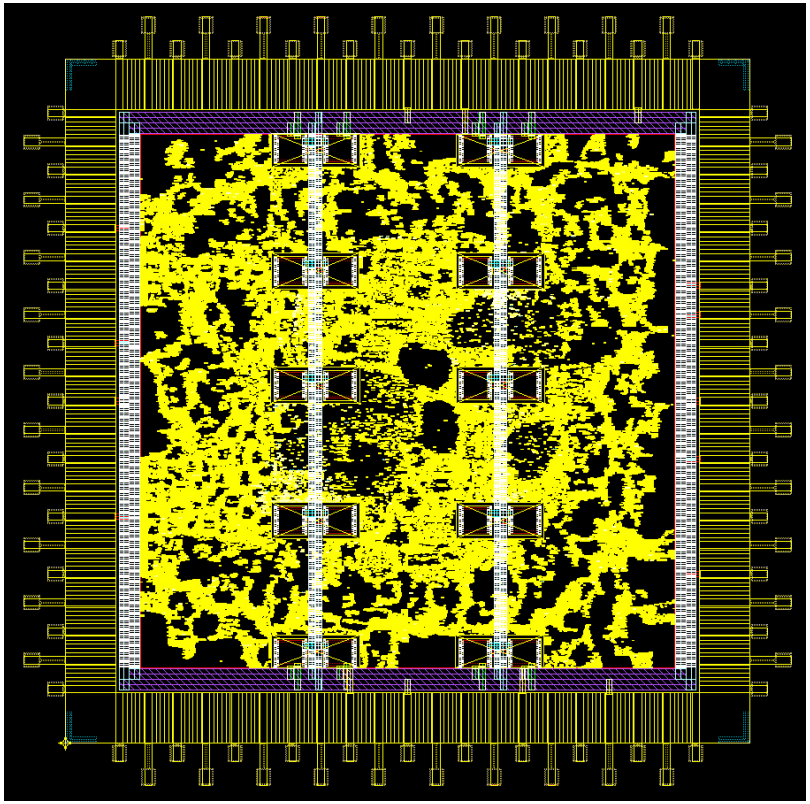


- 會議: **SiPS 2008**
- 期刊: **TVLSI 2011**
- 第八屆旺宏金矽獎-設計組 優勝

Post-layout simulation results

Technology	**TSMC 0.13 μm 1P8M CMOS**
Decoding Algorithm	**EML-MAP**
Decoding Type	**Radix-4 Dual-mode SB/DB**
Window Type	**PW, HW**
Supply Voltage	**1.2 V/3.3 V**
MAX. Frequency	**125 MHz**
Core Size	**1.13 × 1.13 mm^2**
Throughput Rates	**500 Mbps (2PW MAPs)**
	250 Mbps (1HW MAP)
Power	**97.83 mW (2PW MAPs)**
	74.95 mW (1HW MAP)

12-Mode WiMAX CTC Decoder

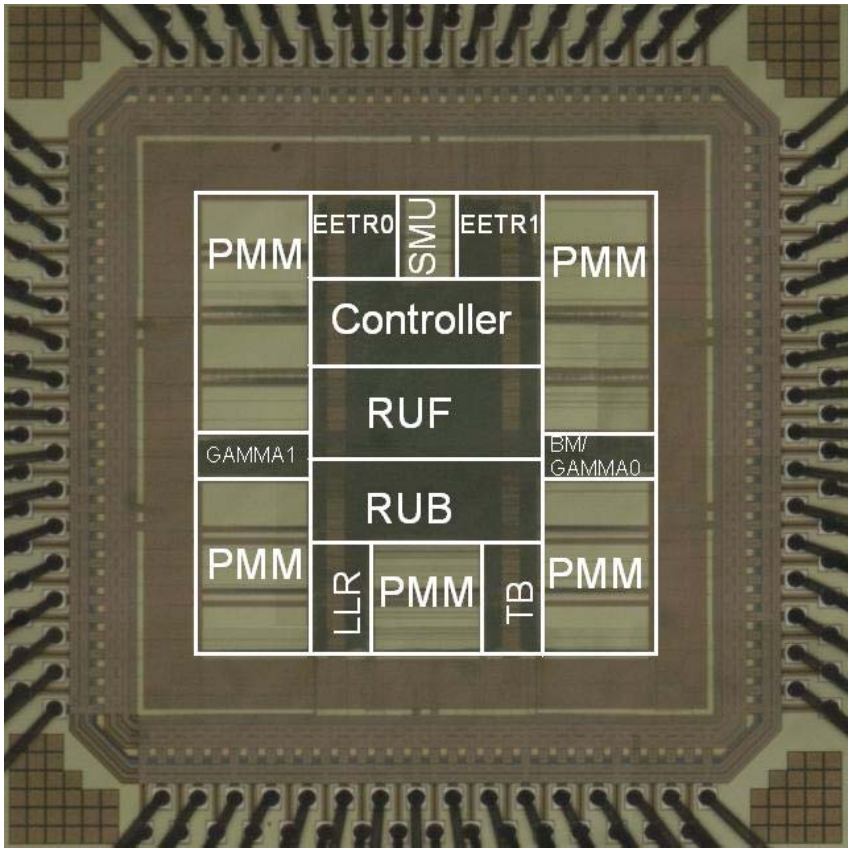


- 會議: **ISCAS 2008, VLSI-DAT 2008**
- 期刊: **TCAS-I 2009**

Post-layout simulation results

Technology	TSMC 0.13μm 1P8M CMOS
Supply Voltage	1.2 V/3.3 V
Decoding Algorithm	EML-MAP
Max. Frequency	100 MHz
Core Size	2.58 x 2.58 mm^2
Max. Power	197.3 mW
Max. Throughput rate @4 Iterations	115.4 Mbps

Triple-Mode MAP/VA IP Design



- 會議: **A-SSCC 2005**
- 期刊: **TVLS-I 2009**
- 第五屆旺宏金矽獎-設計組 最佳創意獎

Measurement results

Technology	**TSMC 0.18um**
Logic Gate	**57.7K**
Supply Voltage	**1.8V**
MAX. Frequency	**100MHz**
Power	**320mW @100MHz**
Die Size	**2.86 x 2.86mm^2**
Single VA	**3.12M bps**
Single MAP	**4.17M bps @6It.**
Concurrent VA/MAP	**1.56M bps(VA) 4.17M bps @6It.(MAP)**